

## WHAT IS CLAIMED IS:

1           1.    An integrated circuit comparator comprising:  
2                    an input receiving an input signal representative  
3 of a difference between quantities to be compared; and  
4                    an input gain stage receiving the input signal  
5 and biased with a pulsed bias current, the input gain stage  
6 producing a gain based upon the input signal.

1           2.    The integrated circuit comparator according to  
2 claim 1, wherein the input signal is a current  
3 representative of transconductance of a differential pair  
4 of input transistors.

1           3.    The integrated circuit comparator according to  
2 claim 1, wherein the input gain stage further comprises a  
3 current source biased by the pulsed bias current and  
4 controlled by the input signal.

1           4.    The integrated circuit comparator according to  
2   claim 1, further comprising:

3               a voltage limiter and a hysteresis circuit  
4   coupled to an output of the input gain stage to reduce  
5   spurious output currents when the pulsed bias current is  
6   not asserted.

1           5.    The integrated circuit comparator according to  
2   claim 4, further comprising:

3               an output gain stage coupled to the hysteresis  
4   circuit and having a gain varying with the gain of the  
5   input gain stage.

1           6.    The integrated circuit comparator according to  
2   claim 4, further comprising:

3               an output gain stage coupled to the hysteresis  
4   circuit and having a fixed gain and a propagation delay  
5   negligible with respect to a propagation delay of the input  
6   gain stage.

1           7.    The integrated circuit comparator according to  
2   claim 1, wherein the pulsed bias current comprises a pulse  
3   at one edge of a system clock and an output of the  
4   comparator is sampled at another edge of the system clock.

1           8.   The integrated circuit comparator according to  
2   claim 1, wherein the comparator selectively operates in a  
3   first mode in which the input gain stage is biased by a  
4   continuous bias current or in a second mode in which the  
5   input gain stage is biased by the pulsed bias current.

1           9. A method of operating an integrated circuit  
2 comparator comprising:

3                 receiving an input signal representative of a  
4 difference between quantities to be compared at an input  
5 for the comparator; and

6                 transmitting the input signal from the input to  
7 an input gain stage biased with a pulsed bias current, the  
8 input gain stage producing a gain based upon the input  
9 signal.

1           10. The method according to claim 9, wherein the  
2 input signal is a current representative of trans-  
3 conductance of a differential pair of input transistors.

1           11. The method according to claim 9, wherein the  
2 input gain stage further comprises a current source biased  
3 by the pulsed bias current and controlled by the input  
4 signal.

1           12. The method according to claim 9, further  
2 comprising:

3                 with an output signal from the input gain stage,  
4 driving a voltage limiter and a hysteresis circuit coupled  
5 to the output of the input gain stage to reduce spurious  
6 output currents when the pulsed bias current is not  
7 asserted.

1           13. The method according to claim 12, further  
2 comprising:

3                 varying a gain of an output gain stage coupled to  
4 the hysteresis circuit with the gain of the input gain  
5 stage.

1           14. The method according to claim 12, further  
2 comprising:

3                 fixing a gain of an output gain stage coupled to  
4 the hysteresis circuit and having a propagation delay  
5 negligible with respect to a propagation delay of the input  
6 gain stage.

1           15. The method according to claim 9, wherein the  
2           pulsed bias current comprises a pulse at one edge of a  
3           system clock and an output of the comparator is sampled at  
4           another edge of the system clock.

1           16. The method according to claim 9, wherein the  
2           comparator selectively operates in a first mode in which  
3           the input gain stage is biased by a continuous bias current  
4           or in a second mode in which the input gain stage is biased  
5           by the pulsed bias current.

1           17. An integrated circuit comprising:

2           a comparator selectively operating in a first  
3       mode in which an input gain stage of the comparator is  
4       biased with a pulsed bias current and a second mode in  
5       which the input gain stage is biased with a continuous bias  
6       current.

1           18. The integrated circuit according to claim 17,  
2       wherein the input gain stage receives an input signal  
3       representative of a difference between quantities to be  
4       compared and produces a gain based upon a current for the  
5       input signal representative of transconductance of a  
6       differential pair of input transistors.

1           19. The integrated circuit according to claim 18,  
2       wherein the input gain stage further comprises a current  
3       source biased by the pulsed or continuous bias current and  
4       controlled by the input signal.

1           20. The integrated circuit according to claim 19,  
2 further comprising:

3               a voltage limiter and a hysteresis circuit  
4 coupled to an output of the input gain stage to reduce  
5 spurious output currents when the pulsed bias current is  
6 not asserted.